

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Hideto OHNUMA

Serial No. 10/053,572

Filed: January 24, 2002

For: METHOD OF MANUFACTURING
SEMICONDUCTOR DEVICE



) Group Art Unit: 2812

) Examiner: J. Kennedy

) CERTIFICATE OF MAILING

) I hereby certify that this correspondence is
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) Commissioner for Patents, P.O. Box 1450,
) Alexandria, VA 22313-1450, on February 16,
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INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. 1.98(a).

Although not written in the abstract, JP 04-290467 discloses a method for forming a poly-Si film over a substrate 11 by CVD, forming a gate insulating film 13 over the poly-Si film by CVD, sputtering, or by heating a surface of the poly-Si film, and doping B- into the poly-Si film through the gate insulating film 13 (see Figure 2).

The examiner's attention is particularly directed to the following documents: U.S. Patent Publication No. 2001/0034089, U.S. Patent No. 6,165,876 and U.S. Patent No. 6,353,244, all to Yamazaki et al.

This Information Disclosure Statement is being submitted with an RCE.
Therefore, no fee is required.

Respectfully submitted,



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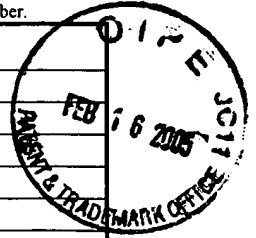
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PTO/SB/08A (08-00)

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if Known		
				Application Number	10/053,572	
Sheet		1	of	2	Filing Date	January 24, 2002
					First Named Inventor	Hideto OHNUMA
					Group Art Unit	2812
					Examiner Name	J. Kennedy
					Attorney Docket Number	0756-2422

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
		2001/0034089		Yamazaki et al.	10/25/2001	
		3,891,468		Ito et al.	06/24/1975	
		4,168,990		Lenie et al.	09/25/1979	
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		5,132,754		Serikawa et al.	07/21/1992	
		5,142,344		Yamazaki	08/25/1992	

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Office ³	Number ⁴	Kind Code ⁵ (if known)			
		JP	03-189626			08/19/1991	Abst.
		JP	04-290467			10/15/1992	Abst.
		JP	04-302147			10/26/1992	Abst.
		JP	05-082552			04/02/1993	Abst.
		JP	10-302707			11/13/1998	Abst.
		JP	64-007559			01/11/1989	Abst.

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Y. MISHIMA et al., <i>Implantation Temperature Effect on Polycrystalline Silicon By Ion Shower Doping</i> , Journal of Applied Physics, Vol. 74, No. 12, December 15, 1993, Pages 7114-7117.	
		S. WOLF, et al., <i>Silicon Processing for the VLSI Era</i> , Vol. 1, January 1, 1986, Pages 175-180, 323-325.	
		H. SCHENK, et al., <i>Polymers for Light Emitting Diodes</i> , Proceedings of the 19 th International Display Research Conference, September 6, 1999, Pages 33-37.	

Examiner Signature	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

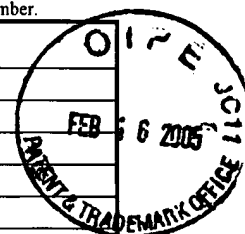
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		Number	Kind Code ² (if known)			
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		6,011,277		Yamazaki	01/04/2000	
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